Jinho Lee

Curriculum Vitae

Assistant Professor
CS, Yonsei University
50, Yonsei-ro, Seoul
Date of birth : 29 Sep., 1986
✉ *leejinho@yonsei.ac.kr*

Research Interests

○ Computer Architecture
- AI acceleration
- Near-data processing

○ Systems for Machine Learning
- Algorithm – Hardware Co-Design
- Distributed Deep Learning

Education

2011 – 2016
Ph.D. Degree, *Seoul National University*, South Korea.
Electrical and Computer Engineering
Advisor: Prof. Kiyoung Choi
Thesis: "Designing Efficient On-chip Networks: Mapping, Management, and Routing"
Graduation: Feb, 2016
GPA: 4.02/4.30

2009 – 2011
M.S. Degree, *Seoul National University*, South Korea.
Electrical Engineering and Computer Science
Advisor: Prof. Kiyoung Choi
Thesis: "Memory-Aware Mapping of Tasks and Communications onto Many Core SoC"
GPA: 4.08/4.30

2005 – 2009
B.S. Degree, *Seoul National University*, South Korea.
Electrical Engineering
GPA: 3.98/4.30
Major GP: 4.08/4.30, Summa cum laude (the highest achievement in university)

Professional Experience

2019 **Assistant Professor (Current),** *CS, Yonsei University*, Accelerated Computing Systems Lab.

2017 **Research Staff Member,** *IBM Austin Research Lab,* Researching graph databases and systems for machine learning.

2016 **PostDoctoral Researcher,** *IBM Austin Research Lab,* Researching graph databases and robotics.

Honors and Fellowship

2011-2013 Global Ph.D. fellowship from National Research Foundation of Korea

2009-2011	Graduate student scholarship from Korea Foundation of Advanced Studies
2005-2009	National scholarship for science and engineering
2005	Top freshmen grand scholarship award from Seoul National University

Conference Publications

2021 Choi, Kanghyun, Deokki Hong, Hojae Yoon, Joonsang Yu, Youngsok Kim, and Jinho Lee (2021). "DANCE: Differentiable Accelerator/Network Co-Exploration". In: *DAC*.

2021 Kim, Heesu, Hanmin Park, Taehyun Kim, Kwanheum Cho, Eojin Lee, Soojung Ryu, Hyuk-Jae Lee, Kiyoung Choi, and Jinho Lee (2021). "GradPIM: A Practical Processing-in-DRAM Architecture for Gradient Descent". In: *HPCA*.

2021 Lee, Jounghoo, Jinwoo Choi, Jaeyeon Kim, Jinho Lee, and Youngsok Kim (2021). "Dataflow Mirroring: Architectural Support for Highly Efficient Fine-Grained Spatial Multitasking on Systolic-Array NPUs". In: *DAC*.

2021 Zhu, Baozhou, Peter Hofstee, Johan Peltenburg, Jinho Lee, and Zaid Al-Ars (2021). "AutoReCon: Neural Architecture Search-based Reconstruction for Data-free Compression". In: *IJCAI*.

2020 Lee, Jinho, Inseok Hwang, Soham Shah, and Minsik Cho (2020). "FlexReduce: Flexible All-reduce for Distributed Deep Learning on Asymmetric Network Topology". In: *DAC*.

2019 Fang, Jian, Jianyu Chen, Jinho Lee, Zaid Al-Ars, and H Peter Hofstee (2019). "Refine and recycle: A method to increase decompression parallelism". In: *ASAP*.

2018 Kang, Bumsoo, Inseok Hwang, Jinho Lee, Seungchul Lee, Taegyeong Lee, Youngjae Chang, and Min Kyung Lee (2018). "My being to your place, your being to my place: Co-present robotic avatars create illusion of living together". In: *MobiSys*.

2017 Fang, Jian, Jinho Lee, Peter Hofstee, and Jan Hidders (2017). "Analyzing In-Memory Hash Join: Granularity Matters." In: *ADMS@ VLDB*, pp. 18–25.

2017 Lee, Jinho, Inseok Hwang, Thomas Hubregtsen, Anne E Gattiker, and Christopher M Durham (2017). "Sci-Fii: Speculative conversational interface framework for incremental inference on modularized services". In: *MDM*.

2017 Vijitbenjaronk, Warut D, Jinho Lee, Toyotaro Suzumura, and Gabriel Tanase (2017). "Scalable time-versioning support for property graph databases". In: *Big Data*.

2016 — Lee, Jinho, Jung Ho Ahn, and Kiyoung Choi (2016). "Buffered compares: Excavating the hidden parallelism inside DRAM architectures with lightweight logic". In: *DATE*.

2015 — Lee, Jinho, Junwhan Ahn, Kiyoung Choi, and Kyungsu Kang (2015). "THOR: Orchestrated thermal management of cores and networks in 3D many-core architectures". In: *ASP-DAC*.

2014 — Han, Sungju, Jinho Lee, and Kiyoung Choi (2014). "Tree-mesh heterogeneous topology for low-latency noc". In: *NocARC*.

2013 — Lee, Jinho and Kiyoung Choi (2013). "A deadlock-free routing algorithm requiring no virtual channel on 3D-NoCs with partial vertical connections". In: *NOCS*.

2013 — Lee, Jinho, Dongwoo Lee, Sunwook Kim, and Kiyoung Choi (2013). "Deflection routing in 3D network-on-chip with TSV serialization". In: *ASP-DAC*.

2012 — Lee, Jinho and Kiyoung Choi (2012). "Memory-aware mapping and scheduling of tasks and communications on many-core SoC". In: *ASP-DAC*.

2012 — Zhu, Mingyang, Jinho Lee, and Kiyoung Choi (2012). "An adaptive routing algorithm for 3D mesh NoC with limited vertical bandwidth". In: *VLSI-SoC*.

2011 — Lee, Jinho, Mingyang Zhu, Kiyoung Choi, Jung Ho Ahn, and Rohit Sharma (2011). "3D network-on-chip with wireless links through inductive coupling". In: *ISOCC*.

Journal Publications

2021 — Kim, Namhyung, Hanmin Park, Dongwoo Lee, Sungbum Kang, Jinho Lee, and Kiyoung Choi (2021). "ComPreEND: Computation Pruning through Predictive Early Negative Detection for ReLU in a Deep Neural Network Accelerator". In: *IEEE TC*.

2021 — Yoo, Mingi, Jaeyong Song, Jounghoo Lee, Namhyung Kim, Youngsok Kim, and Jinho Lee (2021). "Making a Better Use of Caches for GCN Accelerators with Feature Slicing and Automatic Tile Morphing". In: *IEEE CAL*.

2020 — Fang, Jian, Yvo TB Mulder, Jan Hidders, Jinho Lee, and H Peter Hofstee (2020). "In-memory database acceleration on FPGAs: a survey". In: *The VLDB Journal*.

2018 — Kim, Jaehyun, Heesu Kim, Subin Huh, Jinho Lee, and Kiyoung Choi (2018). "Deep neural networks with weighted spikes". In: *Neurocomputing*.

2017 Han, Kyuseung, Jae-Jin Lee, Jinho Lee, Woojoo Lee, and Massoud Pedram (2017). "TEI-NoC: Optimizing ultralow power NoCs exploiting the temperature effect inversion". In: *IEEE TCAD* 37.2, pp. 458–471.

2017 Lee, Jinho, Heesu Kim, Sungjoo Yoo, Kiyoung Choi, H Peter Hofstee, Gi-Joon Nam, Mark R Nutter, and Damir Jamsek (2017). "Extrav: boosting graph processing near storage with a coherent accelerator". In: *pVLDB*.

2015 Lee, Jinho, Kyungsu Kang, and Kiyoung Choi (2015). "Redelf: An energy-efficient deadlock-free routing for 3d nocs with partial vertical connections". In: *ACM JETC*.

2013 Lee, Jinho, Moo-Kyoung Chung, Yeon-Gon Cho, Soojung Ryu, Jung Ho Ahn, and Kiyoung Choi (2013). "Mapping and scheduling of tasks and communications on many-core SoC under local memory constraint". In: *IEEE TCAD*.

Reviews

2014 **Computers & Electrical Engineering,** *Elsevier,* Served as a reviewer for two papers.

2015 **Microprocessors and Microsystems,** *Elsevier,* Served as a reviewer for a paper.

2015 **Transactions on Computer-Aided Design of Integrated Circuits and Systems,** *IEEE,* Served as a reviewer for a paper.

2016 **Microelectronics Journal** *Elsevier,* Served as a reviewer for a paper.

2016 **Design Automation for Embedded Systems** *Springer,* Served as a reviewer for a paper.

2016 **Computer Architecture Letter,** *IEEE,* Served as a reviewer for a paper.

2016 **DAC PhD forum,** Served as a reviewer for four papers.

Languages

English	**Fluent**	*All work performed in English*
Korean	**Native**	*Mother Tongue*